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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,165	08/08/2003	Marc Tremblay	SUN-P9324-SPL	2937

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EXAMINER	
ZHE, MENG YAO	
ART UNIT	**PAPER NUMBER**
2195	
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05/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/637,165	TREMBLAY ET AL.	
	Examiner	Art Unit	
	MENGYAO ZHE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-11, 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-11, 13-20 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-2, 4-11, 13-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claim languages are unclear and indefinite:

i) Claim 1, it is uncertain how "store-marked" of line 10 and "load-marks" of line 16 are related and how they are being used <i.e. are they different marks or the same mark? If different, when does a cache line get store marked and when does it get load-marked? Furthermore, why does the cache line need to clear its load-mark if no previous steps mentioned that it was even marked with a load mark to begin with?>.

Claims 10 and 19 have the same deficiencies as claim 1 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-7, 9-11, 13-16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar et al. Patent No. 7,120,762, 10/10/2006, (hereafter Rajwar) in view of Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution, Ravi Rajwar and James R. Goodman, IEEE, 2001 (hereafter Goodman) further in view of Wang et al., Parent No. 6,006,299 (hereafter Wang).

6. Rajwar was cited in the last office action.

7. As per claims 1, 10, and 19, Rajwar teaches the invention as claimed including a method for executing a commit instruction to facilitate transactional execution on a processor, comprising:

encountering the commit instruction during execution of a program, wherein the commit instruction marks the end of a block of instructions to be executed transactionally; *(Column 3, lines 42-45; Column 7, lines 9-12; the end instruction marks the end of the critical section)*

upon encountering the commit instruction, successfully completing transactional execution of the block of instructions preceding the commit instruction; *(Abstract; Column 7, lines 26-30; Column 9, lines 20-25, lines 45-50; Column 10, lines 45-50)*

wherein changes made during the transactional execution are not committed to the architectural state of the processor until the transactional execution successfully completes. *(Abstract; Column 7, lines 29-33; Column 9, lines 45-50)*

Rajwar does not specifically teach wherein atomically committing changes made during the transactional execution involves: treating store-marked cache lines as locked, thereby causing other processes to wait to access the store-marked cache lines; clearing load marks from cache lines; committing store buffer entries generated during transactional execution to memory, wherein committing each store buffer entry involves unmarking, and thereby unlocking, a corresponding store-marked cache line; and committing register file changes made during transactional execution.

However, Goodman teaches wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution by:

Marking cache lines (Pg 300, left column, Para 2 starting with "If the register checkpoint..." and Para 4: access bit corresponds to marks on the cache line) and treating cache lines as locked, thereby causing other processes to wait to access the store-marked cache lines (Pg 296, Section 3.2, Para 2, starting with "Locks can be elided...";);

committing store buffer entries generated during transactional execution to memory, wherein committing each store buffer entry involves removing previously marked cache lines (Pg 298, left column, the line numbered by 3 "execute critical section speculatively

and buffer results"; Pg 300, Section 5.4, Para 3-4 starting with "When a speculative store is added…");

clearing load-marks from cache lines (Pg 300, left column, Para 2 starting with "If the register checkpoint…" and Para 4: access bit corresponds to load-marks);

committing register file changes made during transactional execution (Pg 299, Section 5.2, sub-section 2. Register checkpoint) all for the purpose of preserving cache coherency during critical section execution.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Rajwar with wherein atomically committing changes made during the transactional execution involves: treating store-marked cache lines as locked, thereby causing other processes to wait to access the store-marked cache lines; clearing load marks from cache lines; committing store buffer entries generated during transactional execution to memory, wherein committing each store buffer entry involves unmarking, and thereby unlocking, a corresponding store-marked cache line; and committing register file changes made during transactional execution, as taught by Goodman, because it allows for cache coherency preservation during critical section execution.

Rajwar in view of Goodman merely teaches locking cache lines but do not specifically teach marking cache lines in order to lock it.

However, Wang teaches marking cached lines for the purpose of locking the cache lines during critical section (Column 2, lines 15-22; Column 10, lines 55-67).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Rajwar in view of Goodman with marking cache lines, as taught by Wang, for the purpose of locking the cache lines during critical section.

8. As per claims 2, 11, 20, Rajwar teaches wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution; and resuming normal non-transactional execution. *(Column 3, lines 15-17; Column 5, lines 57-60; Column 9, lines 45-50)*

9. As per claims 4, 13, Rajwar teaches
wherein if an interfering data access from another process is encountered during the transactional execution and prior to encountering the commit instruction, the method further comprises: discarding changes made during the transactional execution; and attempting to re-execute the block of instructions. *(Column 8, lines 50-65)*

10. As per claims 5, 14, Rajwar teaches
wherein for a variation of the commit instruction, successfully completing the transactional execution involves: atomically committing changes made during the transactional execution; and commencing transactional execution of the block of

instructions following the commit instruction. *(Abstract and Column 9, lines 45-50, Column 3, line 15-17)*

11. As per claims 6, 15, Rajwar teaches

wherein potentially interfering data accesses from other processes are allowed to proceed during the transactional execution of the block of instructions. *(Column 2, lines 47-50)*

12. As per claims 7, 16, Rajwar teaches wherein the block of instructions to be executed transactionally comprises a critical section *(Column 2, lines 47-50)*

13. As per claims 9, 18, Rajwar teaches wherein the commit instruction is defined in a platform-independent programming language *(Column 10, lines 8-15)*

14. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar et al. Patent No. 7,120,762, 10/10/2006, (hereafter Rajwar) in view of Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution, Ravi Rajwar and James R. Goodman, IEEE, 2001 (hereafter Goodman) further in view of Wang et al., Parent No. 6,006,299 (hereafter Wang) further in view of Hecht et al, Pub. No. US 2003/0064808 (hereafter Hecht).

15. Hecht was cited in the last office action.

16. As per claims 8, 17, Rajwar teaches that the invention as he disclosed may be used on different computer architecture, meaning that they can be platform independent *(Column 10, lines 8-15)*

Rajwar does not teach the commit instruction being platform dependent. However, Hecht teaches a

converter program that converts platform independent programs into platform dependent programs for the purpose of running the program on a specific type of machine *(Paragraph 14)*

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the invention of Rajwar with

Converting the platform independent instruction to platform dependent instruction,

as taught by Hecht, because it allows the program to run on a specific type of machine.

Response to Arguments

17. Applicant's argument filed on 2/19/2008 regarding claims 1-2, 4-11, 13-20 have been fully considered but they are moot in view of new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-

6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195